The 3D Silicon Leader

RF companion chip based on PICS technology for small and reliable medical device packaging:

Application to Ultra-Low Power RF Implants

Mohamed Mehdi Jatlaoui, Sébastien Leruez, Olivier Gaborieau, Catherine Bunel

2016.05.03

Outline

- Introduction

- Silicon interposer for medical applications
  - PICS silicon interposer
  - Medical devices with IPDiA inside
  - Implantable RF module

- Full RF Module integration: 3 design win
  - IPD RF interposer + TSV
  - IPD RF interposer + transceiver (bare die)
  - IPD RF interposer + embedded transceiver between PCB laminates
  - PICS technology benefits

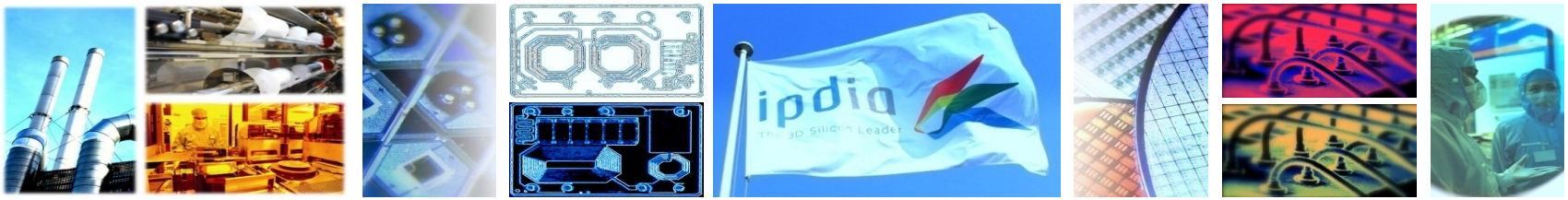
- Conclusions

Who are we?

ipdia
The 3D Silicon Leader

Who are we?

- Independent High-Tech company located in Caen, Normandy, France
- Dedicated to manufacturing of leading edge Integrated Passive Devices (PICS)
- 116 people and operating own silicon 6” wafer fab
- Strong R&D team collaborating with leading research institutes
- Technology adopted by 3 of the top 5 leaders in medical electronics as well as by key players in the semiconductor area and HI-Rel industry



Quality Certifications

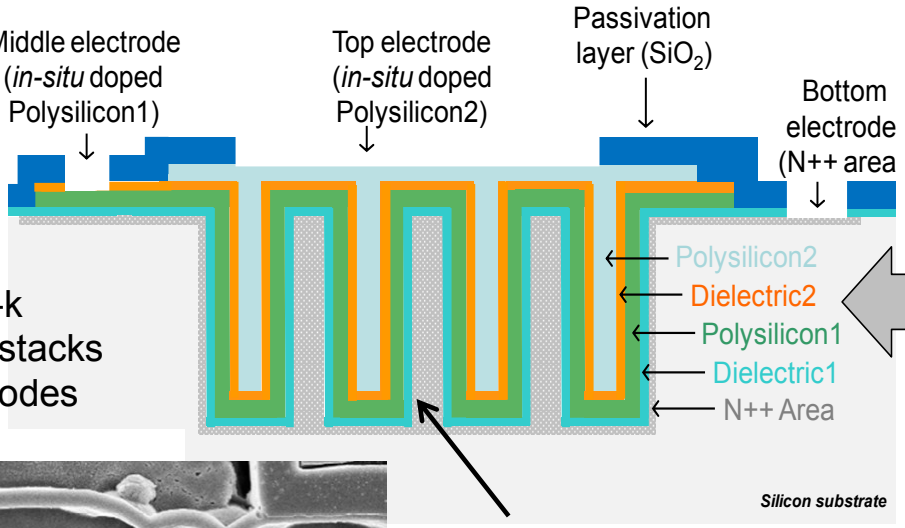
“We aim at exceeding our customers expectations by reaching the highest level of Quality Standards”

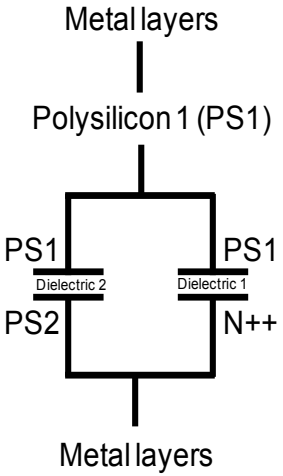
Franck Murray, IPDiA C.E.O.

- ISO-9001
- ISO-14001
- ISO-TS16949 (Automotive)
- ISO-13485 (Medical)
- OHSAS-18001
- RoHS compliant
- AEO (Authorised Economic Operator)

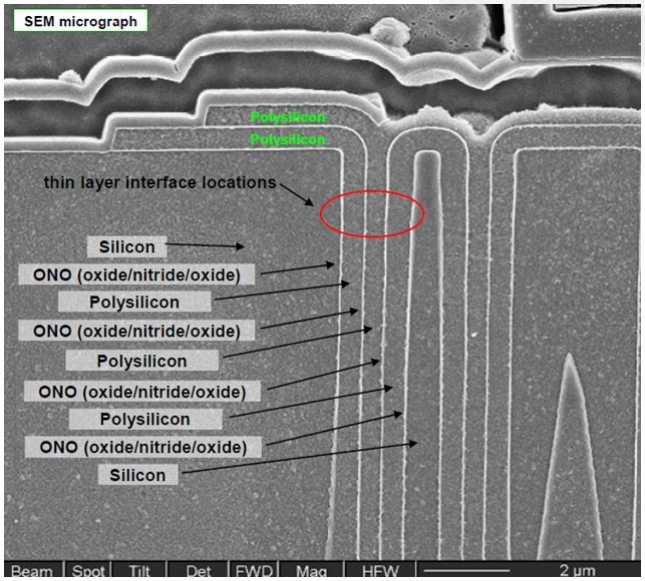
3D structure

2 parallelized capacitors in a MIMIM architecture to increase the capacitance value

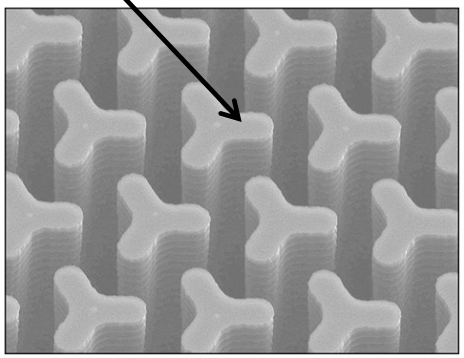


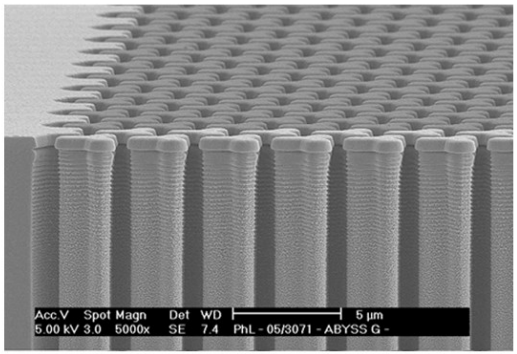


Based on high-k materials nanostacks & barrier electrodes



Tripod



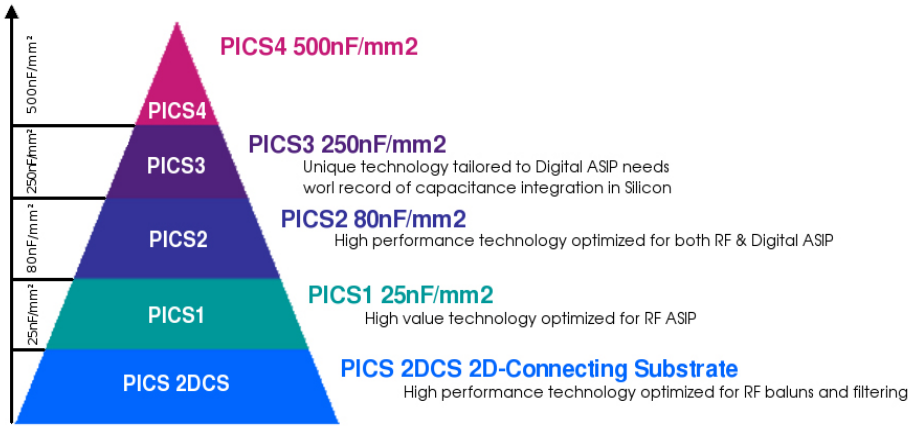


Tilted SEM view

PICS – 3D cap component overview

- **3D Silicon capacitors**

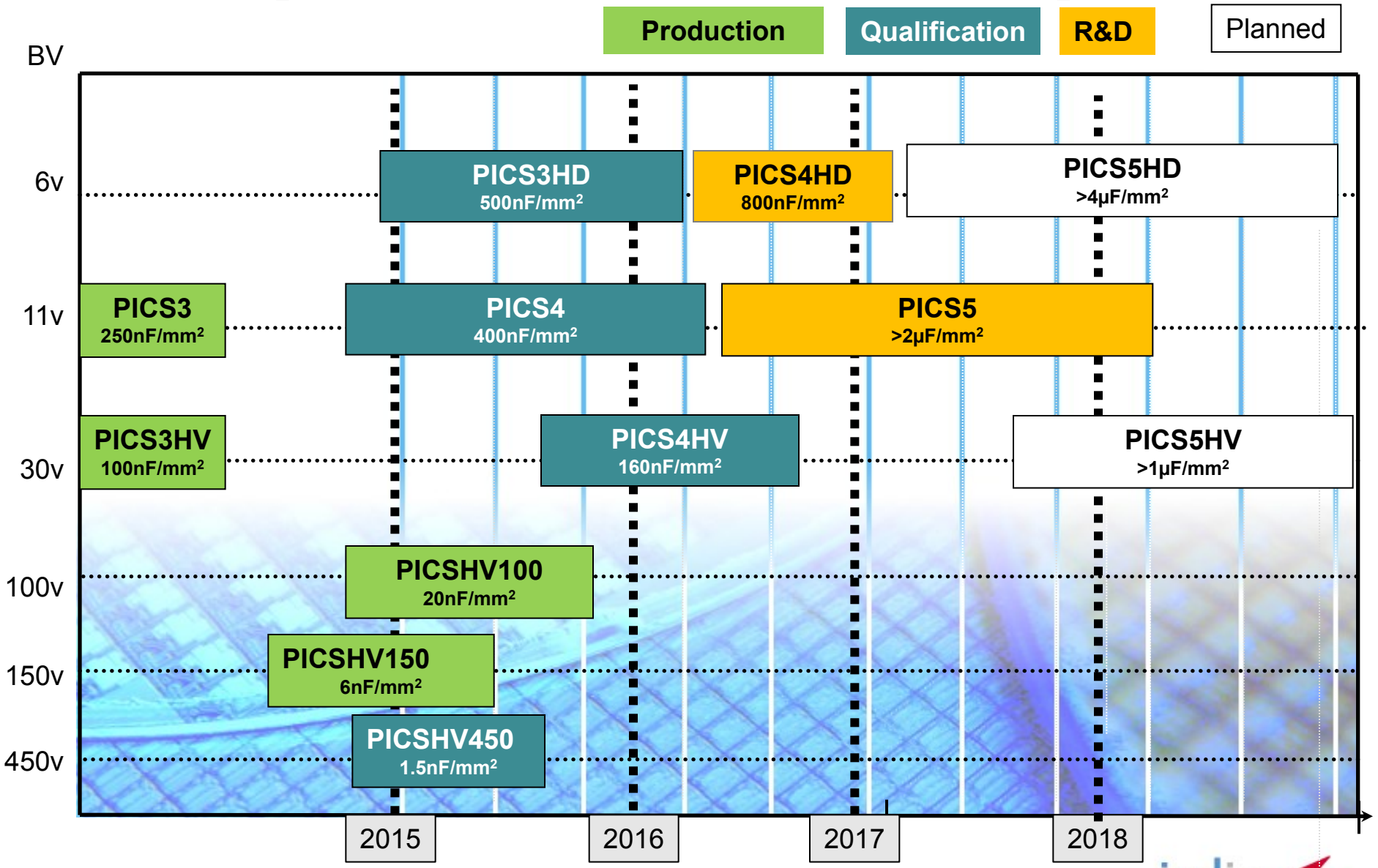
  - **5 PICS platforms available**
    - *Capacitance density up to 500nF/mm²*
    - *Low Profile (down to 80µm)*
    - *Low ESR / Low ESL specific structures*



  - **Voltage rating**
    - *Breakdown voltage from 5 to 500V*
    - *High dielectric isolation typ. <1nA/mm² (25° C/VUse)*
    - *Temp linearity <100ppm/K*
    - *Voltage linearity <100ppm/V*

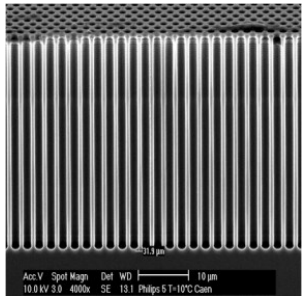
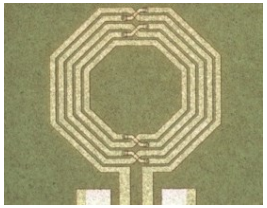
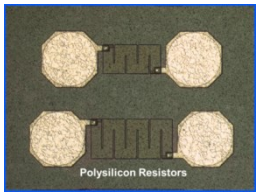
  - **Reliability**
    - *> 10 yrs @ operating voltage @ 100° C*
    - *FIT (Failure in Time) below 1 at 225° C*
    - *Mechanical shock tests*
    - *Thermal cycling tests : up to 3000 cycles in std conditions and 330 cycles in harsh conditions*

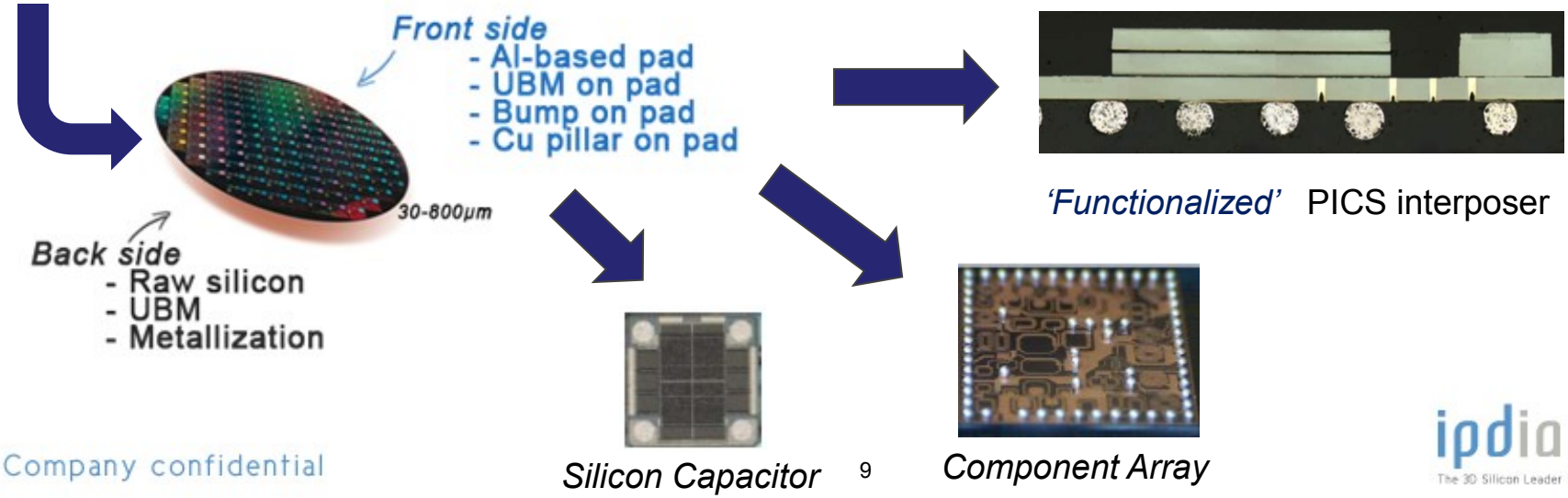
3D Capacitor Global Roadmap



IPDiA terminology

– PICS (Passive Integrated Connective Substrate) technology

3D capacitors (trench Capacitors)	MIM Capacitors	Inductors	Polysilicon Resistors	TSVs	Diodes
	80pF/mm² Matching <1%				
		Up to 3 metal Top metal > 10um Superior Q	*Matchnig < 0.5%* *800 Ω/□* MΩ resistor / mm²		Surge protection ESD / OVS



Silicon Interposer for medical applications

ipdia
The 3D Silicon Leader

PICS Silicon-Interposer, generals

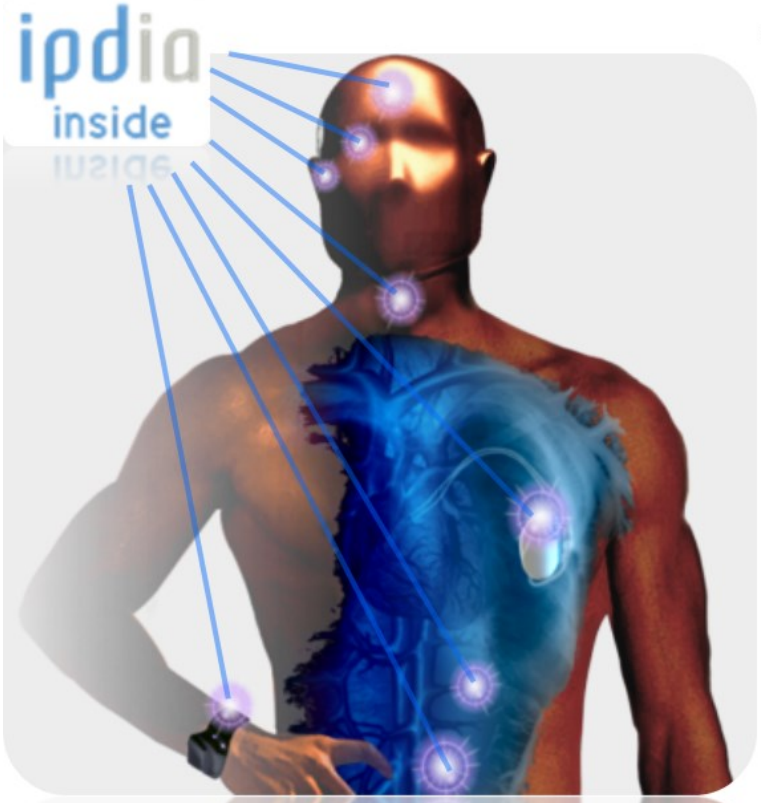
- **Integration of passive component (Wafer processing)**
  - To build /adapt a full system module (adding Passives and Diodes)
  - To miniaturize the system thanks to PICS form factor & performances

- **A platform to receive external components (Chip-to-Wafer processing)**
  - External IC's in picked & placed or flipped technologies
  - SMD's or discrete packages in surface mount technology

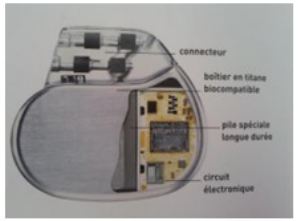
- **To interconnect integrated passives & external components (2D-interposer)**
  - Interconnection factor prepared from packages to advanced IC's
  - Interconnection dimensions thanks to wafer processing
  - Optimized performances thanks to small interconnection dimension

- **To interconnect top and bottom sides (3D-interposer)**
  - Conductive vias (Wafer processing)
  - Double-side patterning process (Various metal finishing options)

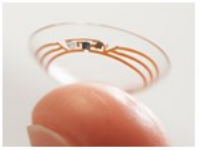
Medical Devices with IPDiA inside



- Implantable Devices
  - Cardiac area: PICS technology can replace 10 to 50 passive components
  - External/Internal Implant: cochlear implant, eye implant, hearing aid, monitoring
  - Deep brain stimulation: extreme miniaturization

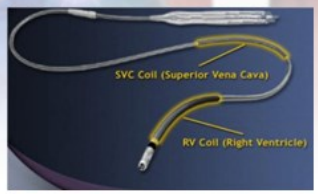


Cardiac rhythm management

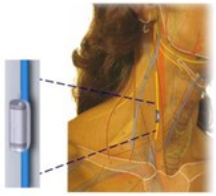


Eye care implant

Medical Sensor



Learning pacing



Neuro-stimulation modulation

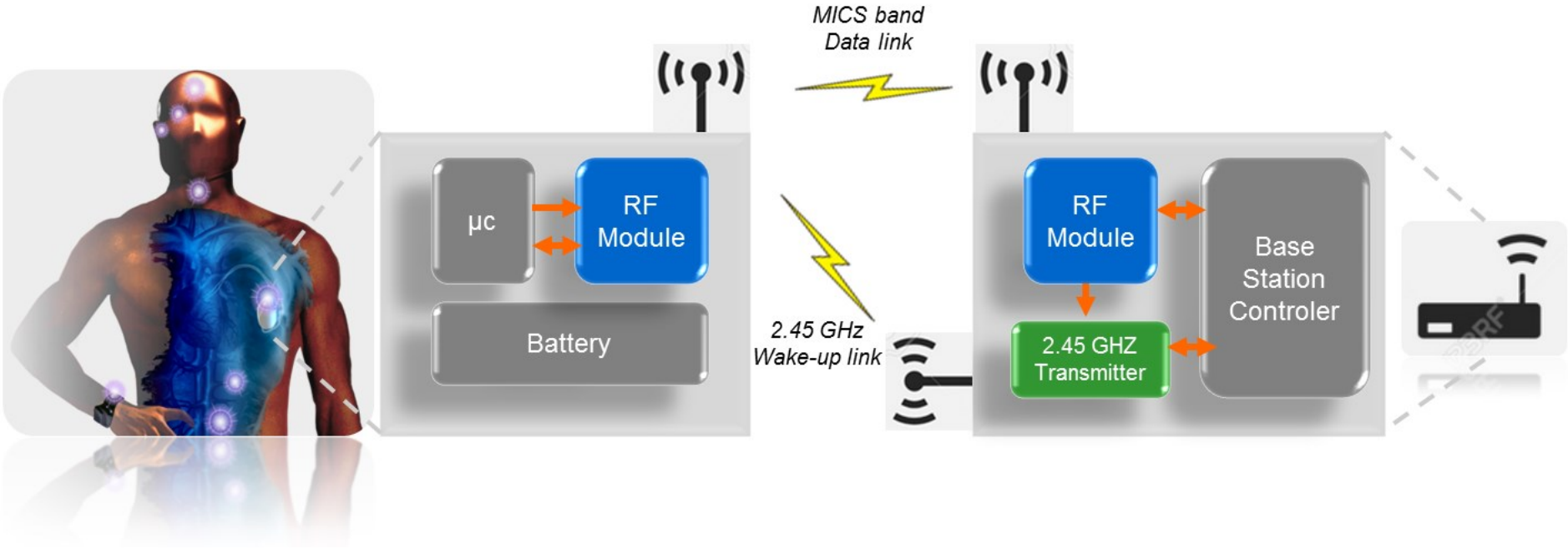
Pain relief

Hearing aid
Cochlear implants

ipdia
The 3D Silicon Leader

Implantable RF Module (MICS, ISM)

- The target is to integrate a full RF module based on PICS interposer



- MICS = Medical Implant Communications Service (402 - 405 MHz): Implant to instrument Tx/Rx
- ISM = Industriel, Scientific and Medical Radio Frequency band
- Advanced packaging technology can deliver substantial space and volume savings
- Extreme miniaturization in all three axis

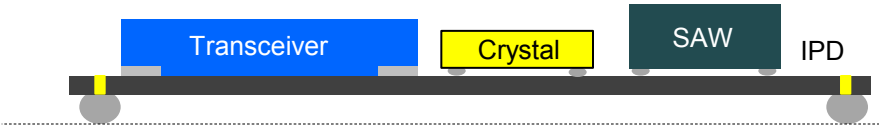
Full RF module integration: 3 design win

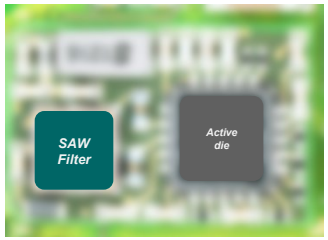
ipdia
The 3D Silicon Leader

Full RF Module integration_Config 1

- *Integration technology*:
  - PICS2C TSV (80nF/mm² - through silicon vias – copper interconnect - 3.6V max operating voltage)

- *Packaging technology*:
  - WLCSP
  - Die size :
    7x10.5 mm (~73.5mm2)
    28 pads (with 1mm pitch)
  - Interconnection
    1st interco = 400um / SnPb
    2nd interco = Solder printing (SAC305)
  - 5 components (Transceiver, SAW, Crystal, Ferrite, Diode)
  - Stack thickness ~ 2mm max
  - PICS target thickness 200um, component Max thickness 1250um

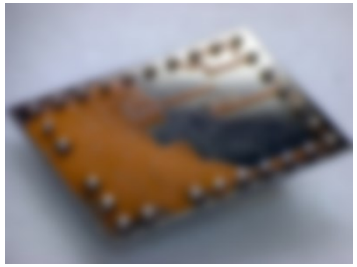




SMD & PCB Technology

PICS Technology

- *Performances*:
  - PICS capacitors : +/-15% accuracy, matching <0.2%
  - Resistors : +/-15% accuracy, matching <0.2%
  - Excellent temperature and voltage stability for PICS and MIM capacitors

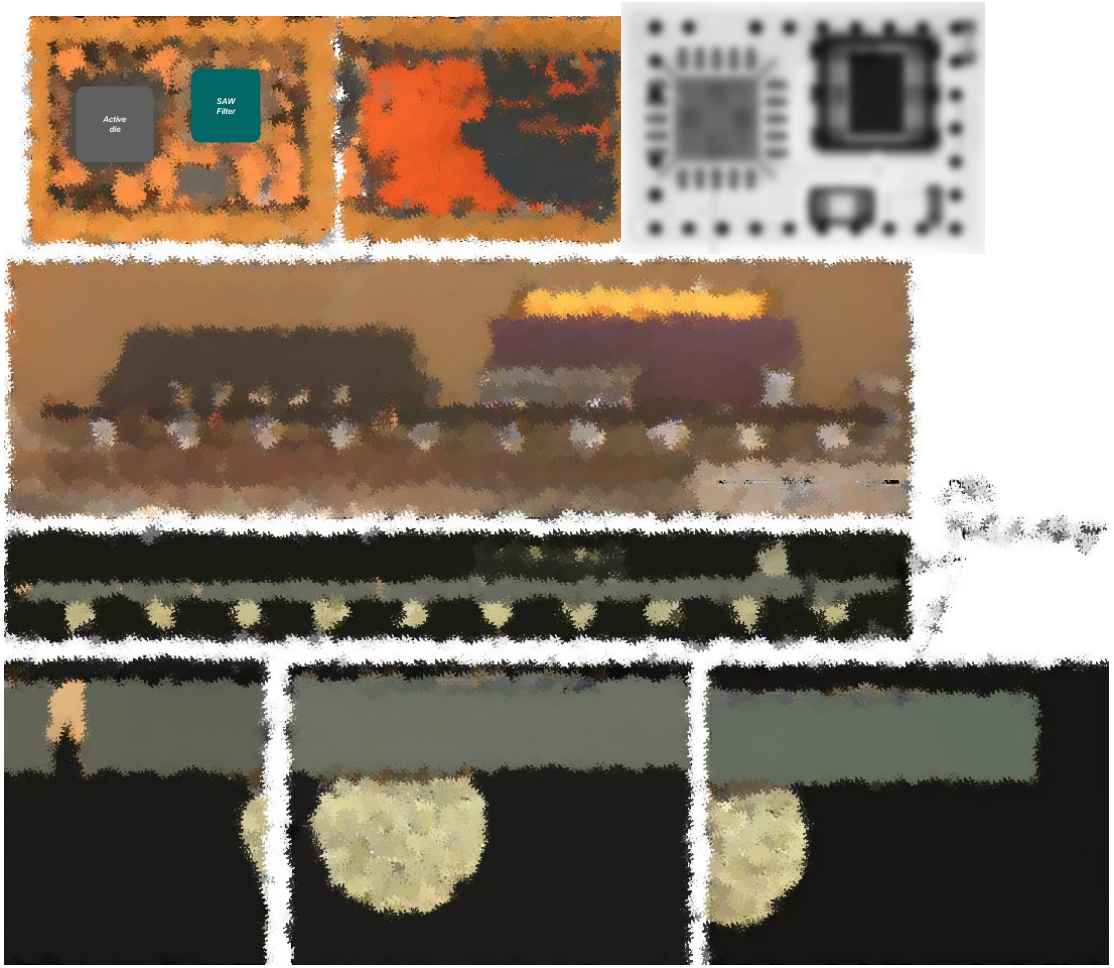

Back Side Overview

Remarks
- Cu RDL, NiAu UBM, SnPb solder balls, soldering on PCB
- Underfill required BTW active die and PICS interposer


Cross section Overview

Full RF Module integration_Config 1

- **Decoupling part + power supply**
  - Decoupling capacitor are placed as close as possible to the Pin to protect
  - Traces are large enough for overall current consumption and control voltage drop to active circuit
- **GND plane**
  - Separate RF_GND and Digital_GND
- **RF path (saw filter + matching networks + ESD diode)**
  - EM Simulations to validate RF performances
  - Ensure no cross talk with other blocks
- **Sensitive part (xtal connections)**
  - shielding/guard-ring to avoid signal coupling noise from aggressor block
- **Aggressive part : data bus**
  - Physical separation between aggressive blocks and sensitive / RF part
  - Use shielding/guard-ring to contain signal propagation to substrate
  - Optimized native diode to substrate

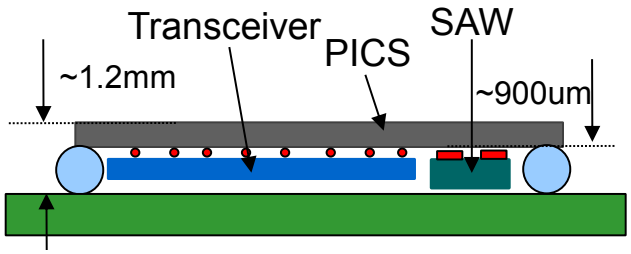


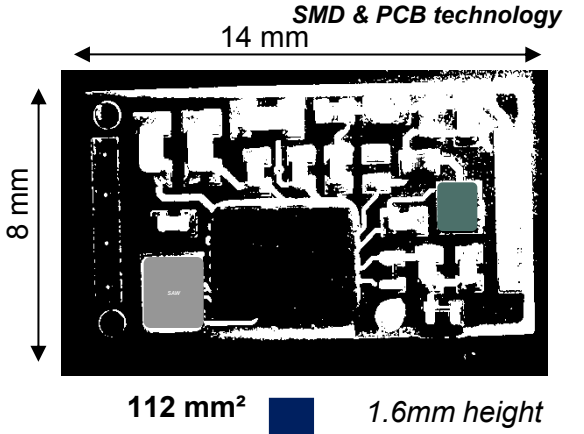
Full RF Module integration_Config 2

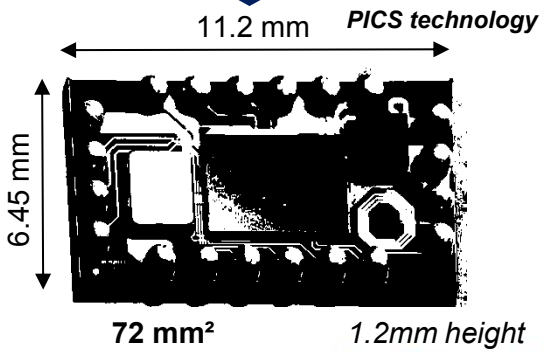
- *Integration technology*:
  - PICS2C (80nF/mm² - copper interconnect - 3.6V max operating voltage).
- *Packaging technology*:
  - WLCSP
  - Die size :
    6.45x11.2 mm (~72.3mm2)
    20 pads
  - Interconnection
    1st interco = 890um / 1.27mm pitch, solder ball (SAC305)
    2nd interco = 40um standoff /~135um pitch, copper pillar technology
  - 3 components (Transceiver, SAW, Crystal)
  - Stack thickness ~ 1.2mm max
  - PICS target thickness 300um, component Max thickness 600um
- *Performances*:
  - PICS capacitors : +/-15% accuracy, matching <0.2%
  - Resistors : +/-15% accuracy, matching <0.2%
  - Excellent temperature and voltage stability for PICS and MIM capacitors.

Remarks

- Underfill required BTW active die and PICS interposer





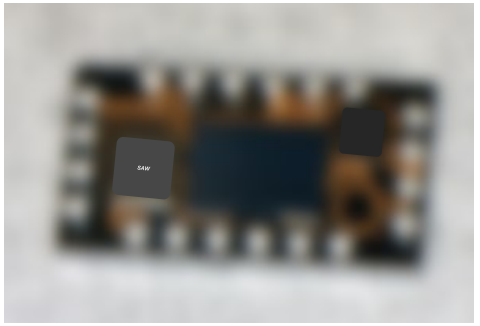


↘ *36 % area decrease !*

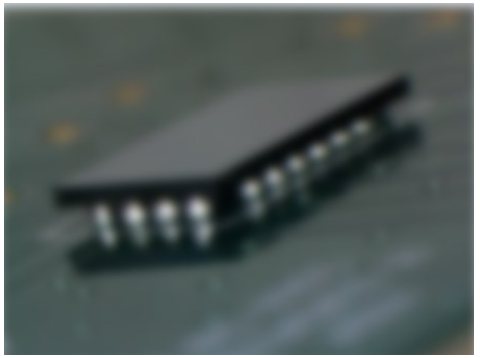
↘ *25 % height decrease !*

Full RF Module integration_Config 2

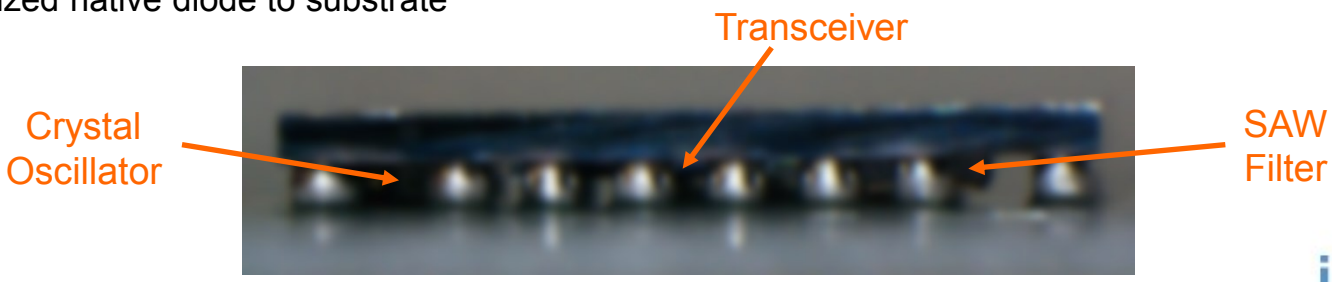
- **Decoupling part + power supply**
  - Decoupling capacitor are placed as close as possible to the Pin to protect
  - Traces are large enough for overall current consumption and control voltage drop to active circuit
- **GND plane**
  - Separate RF_GND and Digital_GND
- **RF path (saw filter + matching networks)**
  - EM Simulations to validate RF performances
  - 400MHz & 2.4GHz Matching network
  - 20 nH @ 400M / Q = 26 / 2.3 ohms with GND (PCB) / SRF > 1G
  - 3.8 nH @ 2G45 / Q=48 / 1.2 ohms with GND (PCB) / SRF > 7G
- **Sensitive part (xtal connections)**
  - shielding/guard-ring to avoid signal coupling noise from aggressor block
- **Aggressive part : data bus**
  - Physical separation between aggressive blocks and sensitive / RF part
  - Use shielding/guard-ring to contain signal propagation to substrate
  - Optimized native diode to substrate



RF module before soldering



RF module soldered by flip chip onto PCB

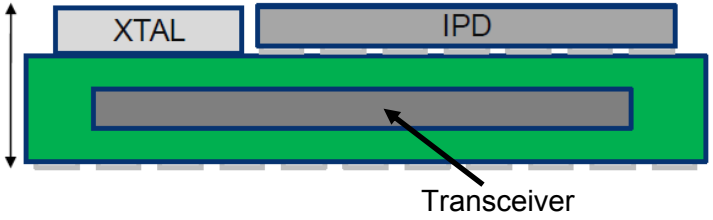


Full RF Module integration_Config 3

- *Integration technology*:
  - PICS3C (250nF/mm² - 80pF/mm² MIM capacitors – Top metal layer: copper 5.5µm thick - 3.6V max operating voltage).
  - Embedded transceiver die between PCB laminations

- *Packaging technology*:
  - WLCSP
  - Die size : original size = *12x6 mm*
    Current Module = 5.5x4.5.5 mm (~25mm2) / IPD = 3.2x4 mm
    28 pads (with 500um pitch)
  - Interconnection
    Ball dropping = 200um / 1.27mm pitch, solder spheres (SAC305)
  - No SMD on the IPD
  - Stack thickness: Module = 1 mm max
  - PICS target thickness 245um

Module height
1mm Maximum



PICS Technology

- *Performances*:
  - PICS capacitors : +/-15% accuracy, matching <0.2%
  - Resistors : +/-15% accuracy, matching <0.2%
  - Excellent temperature and voltage stability for PICS and MIM capacitors.

Remarks

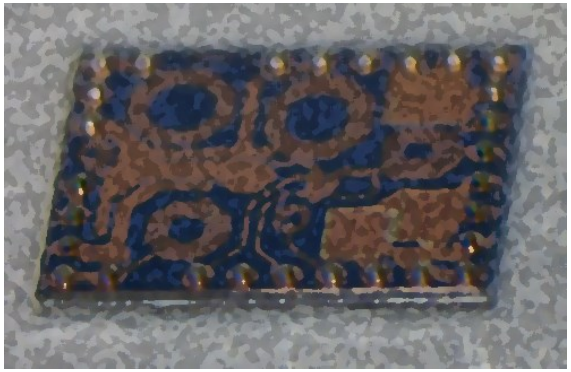
- Underfill required BTW IPD and PCB interposer

Full RF Module integration_Config 3

- **Decoupling part + power supply**
  - Decoupling capacitor are placed as close as possible to the Pin to protect
  - Traces are large enough for overall current consumption and control voltage drop to active circuit

- **GND plane**
  - Separate RF_GND and Digital_GND

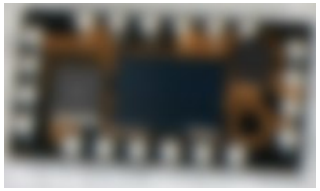
- **RF part (saw filter + matching networks)**
  - EM Simulations to validate RF performances
  - 400MHz & 2.4GHz Matching network
  - 60nH @ 403M / Q = 19 / 7.3 ohms with GND (PCB) / SRF > 1.5G
  - 10.5 nH @ 2G45 / Q= 30 / 5.5 ohms with GND (PCB) / SRF > 6G



RF companion chip ready to be flip-chipped onto PCB

PICS technology benefits

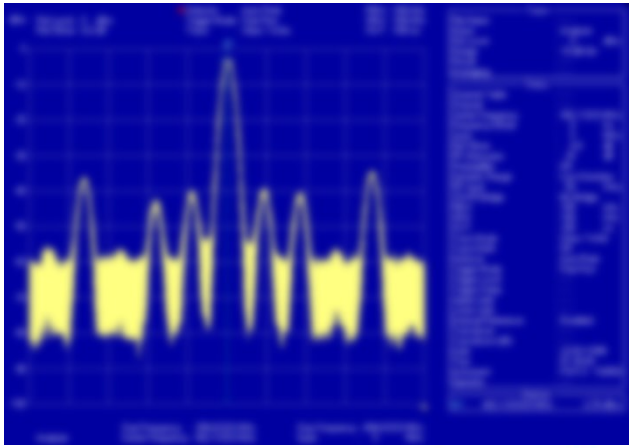
Config 1



Config 2

Config 3

- Toward ***'hidden'*** die technology
- RF front end integration showing improved performances (in terms of Tx output power and Rx sensitivity) in a small size with an excellent gain conversion, a high filter rejection and an efficient decoupling
- Simplified assembly process: cheaper and faster (1 x IPD i/o 15 minimum)
- Better **RF performances and robustness**
- Improvement of **temperature and voltage stability**
- More **reliable** than discrete components
- Significant **size reduction** can be achieved by reducing SAW filter dimensions for example
- Test:
  - Wafer probe test before TSV making
  - TSV continuity thanks to dedicated structures
  - XRay analysis
  - Electrical test on final module
  - RF wireless test
- Simulations and measurements match pretty well



Conclusions

ipdia
The 3D Silicon Leader

Conclusions

- New integration approach: more than just replacing discrete components → IPDiA passive integration technology coupled with 2D/3D interposers bring differentiations and amazing miniaturization
- Medical devices are both using some recent progresses of our industry and driving our industry into new directions → learning is priceless
- Unique know-how: design abilities, packaging investigations and close collaboration with our customers → Customized Design & Customized Process
- Technology already qualified and manufactured for medical implants and high Rel markets
- Intrinsic higher reliability (vs. SMDs) and lifetime (low leakage)
- Fully compatible with different kinds of assembly processes (IC, SMD…)
- Fully functional in the application

Thanks for your attention

mohamed.jatlaoui@ipdia.com